Claims

1. A memory device, comprising:

a substrate;

a plurality of self-aligned nano-rectifying elements, having:

a plurality of first electrode lines disposed over said substrate,

a plurality of device structures disposed on said plurality of first electrode lines forming said plurality of self-aligned nano-rectifying elements, each device structure having at least one lateral dimension less than about 75 nanometers;

a plurality of switching elements, said switching elements disposed over and self-aligned in at least one direction with said device structures; and

a plurality of second electrode lines disposed over, electrically coupled to, and self-aligned to said switching elements, whereby a memory device is formed.

2. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of first semiconductor lines including a dopant of a first polarity.

3. The memory device in accordance with claim 2, wherein said plurality of first semiconductor lines further comprises a plurality of first epitaxial semiconductor lines.

4. The memory device in accordance with claim 2, wherein said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant of a second polarity, wherein each semiconductor device structure forms a semiconductor junction with one of said plurality of first semiconductor lines, said semiconductor junction having an area with at least one lateral dimension less than about 75 nanometers.

5. The memory device in accordance with claim 2, wherein said plurality of semiconductor device structures further comprises a plurality of epitaxial semiconductor device structures.

6. The memory device in accordance with claim 2, wherein each device structure of said plurality of device structures further comprises:

an intrinsic semiconductor structure disposed on one of said plurality of first semiconductor lines; and

a second semiconductor device structure including a dopant of a second polarity, disposed on said intrinsic semiconductor structure, wherein said intrinsic semiconductor structure and said second semiconductor device structure each have at least one lateral dimension less than about 75 nanometers, whereby a plurality of p-i-n diode elements are formed.

7. The memory device in accordance with claim 2, wherein said plurality of first semiconductor lines is formed on an insulating layer formed on said substrate.

8. The memory device in accordance with claim 7, wherein said insulating layer is selected from the group consisting of SiOx, SixNy, SiOxNy, SixCy, and mixtures thereof.

9. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of metal electrode lines, and wherein said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant, forming a plurality of Schottky barrier contacts between said plurality of metal electrode lines and said plurality of semiconductor device structures, each Schottky barrier contact having an area with at least one lateral dimension less than about 75 nanometers.

10. The memory device in accordance with claim 1, wherein said plurality of first electrode lines further comprises a plurality of metal electrode lines, and wherein each device structure further comprises:

a dielectric layer disposed on one of said plurality of metal electrode lines; and

a metal layer disposed on said dielectric layer, forming a plurality of metal-insulator-metal rectifying elements, wherein each metal-insulator-metal rectifying element having at least one lateral dimension less than about 75 nanometers.

11. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a ferroelectric material.

12. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a phase change material.

13. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a filament forming material.

14. The memory device in accordance with claim 13, wherein said filament forming material is selected from the group consisting of As_2Se_3:Ag, Cu_2S, InSe, and mixtures thereof.

15. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises an organic or polymer layer.

16. The memory device in accordance with claim 15, wherein said organic layer further comprises a self-assembled monolayer of organic molecules.

17. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a piezoelectric material.

18. The memory device in accordance with claim 1, wherein each switching element of said plurality of switching elements further comprises a chalcogenide material.

19. The memory device in accordance with claim 1, wherein said plurality of first electrode lines are substantially parallel to each other.

20. The memory device in accordance with claim 19, wherein said plurality of switching elements further comprises a plurality of switching lines substantially parallel to each other.

21. The memory device in accordance with claim 20, wherein said plurality of switching lines are substantially mutually orthogonal to said plurality of first electrode lines.

22. The memory device in accordance with claim 1, wherein each device structure has an area less than about 5,625 square nanometers.

23. A memory device, comprising:

a substrate;

a first plurality of conductive lines substantially parallel to each other disposed on said substrate;

a plurality of semiconducting junctions formed on said first plurality of conductive lines, said junctions having at least one lateral dimension less than about 75 nanometers;

a second plurality of conductive lines substantially parallel to each other and substantially mutually orthogonal to said plurality of semiconducting lines; and

a storage media disposed between said first and said second conductive lines and electrically coupled to said junctions and said second plurality of conductive lines.

24. A memory device comprising:

a substrate;

means for rectifying including a first plurality of conductive lines substantially parallel to each other disposed on said substrate, said means for rectifying self-aligned with said plurality of conductive lines, wherein said means for rectifying having at least one lateral dimension less than about 75 nanometers;

means for storing a data bit in each of a plurality of storage elements disposed over said first plurality of conductive lines and self-aligned to said means for rectifying; and

means for electrically addressing said plurality of storage elements, wherein each storage element self-aligned with said means for electrically addressing, and wherein each intersection of said means for electrically addressing and said first plurality of conductive lines defines a logic cell, of a memory structure.

25. A memory device, comprising:

a substrate;

a plurality of rectifying structures, disposed on said substrate, said rectifying structures form an i x j array, wherein i and j are integer values, each rectifying structure having at least one lateral dimension less than about 75 nanometers;

a plurality of storage media elements, each storage media element disposed on and electrically coupled to one of said rectifying structures, each storage media element having at least one lateral dimension less than about 75 nanometers; and

a plurality of electrical conductor lines disposed on and electrically coupled to said plurality of storage media elements, wherein each storage media element is self-aligned to one of said rectifying structures and is self-aligned to one of said electrical conductor lines.

26. A memory device, comprising:

a substrate;

a plurality of self-aligned nano-rectifying elements, having:

a plurality of first conductive lines disposed over said substrate, each first conductive line having at least one lateral dimension less than about 75 nanometers,

a plurality of device structures disposed on said plurality of first conductive lines, each device structure having at least one lateral dimension less than about 75 nanometers, wherein the combination of said first conductive lines and said device structures forms said plurality of nano-rectifying elements;

a plurality of switching elements, each switching element disposed on and electrically coupled to one of said plurality of device structures; and

a plurality of second conductive lines, said second conductive lines electrically coupled to said plurality of switching elements, each second conductive line intersects with at least one first conductive line, wherein each

nano-rectifying element is substantially facially coextensive, coincident, and coplanar with one of said plurality of first conductive lines and one of said plurality of switching elements.

27. A memory device, comprising:

a substrate;

a plurality of semiconducting lines including a dopant of a first polarity said semiconducting lines substantially parallel to each other and disposed over said substrate;

a plurality of semiconducting structures including a dopant of a second polarity disposed on said plurality of semiconducting lines;

a plurality of junctions formed between said lines and said semiconducting structures said junctions having at least one lateral dimension less than about 75 nanometers;

a switching element disposed on and electrically coupled to said semiconducting structures; and

a plurality of electrical conductors substantially parallel to each other, coupled to said storage media and substantially mutually orthogonal to said plurality of semiconducting lines.

28. A method for manufacturing a cross-bar device, comprising:

nano-imprinting a first nano-imprinting layer disposed over a device structure layer, said device structure layer disposed over a first addressable layer, said first addressable layer disposed over a substrate;

forming a plurality of self-aligned nano-rectifying elements from said first addressable layer and said device structure layer, each rectifying element having at least one lateral dimension less than about 75 nanometers;

nano-imprinting a second nano-imprinting layer disposed over an electrically conductive layer, disposed over a storage media layer, said storage media layer disposed on said plurality of nano-rectifying elements; and

forming a plurality of self-aligned nano-storage structures, each storage structure having at least one lateral dimension less than about 75 nanometers.

29. The method in accordance with claim 28, wherein nano-imprinting said first nano-imprinting layer further comprises urging a nanoimprinter toward said first nano-imprinting layer.

30. The method in accordance with claim 29, further comprising exposing said first nano-imprinting layer to a predetermined exposure of ultraviolet radiation through an ultraviolet transmitting nanoimprinter having a transmittance in the wavelength range from about 250 nm to about 500 nm.

31. The method in accordance with claim 28, further comprising:

creating a first addressable layer over said substrate; and

creating a device structure layer disposed over and electrically coupled to said first addressable layer.

32. The method in accordance with claim 31, wherein creating said first addressable layer further comprises creating a first epitaxial semiconductor layer, including a dopant of a first polarity, over said substrate; and wherein creating said device structure layer further comprises creating a second epitaxial semiconductor layer, including a dopant of a second polarity, over said first epitaxial semiconductor layer.

33. The method in accordance with claim 32, further comprising creating a dielectric layer disposed between said first epitaxial semiconductor layer and said substrate.

34. The method in accordance with claim 32, further comprising creating an intrinsic semiconductor layer disposed between said first and said second epitaxial semiconductor layers.

35. The method in accordance with claim 31, wherein creating said first addressable layer further comprises creating a first metal layer disposed over said substrate.

36. The method in accordance with claim 35, further comprising creating a dielectric layer on said first metal layer, and wherein creating said device structure layer further comprises creating a second metal layer disposed on said dielectric layer.

37. The method in accordance with claim 35, further comprising creating a semiconductor layer having a dopant, said semiconductor layer electrically coupled to said first metal layer forming a Schottky barrier contact.

38. The method in accordance with claim 30, wherein creating a first addressable layer further comprises creating a doped polysilicon layer.

39. The method in accordance with claim 30, wherein creating a device structure layer further comprises creating a doped polysilicon layer.

40. The method in accordance with claim 28, wherein forming a plurality of self-aligned nano-rectifying elements further comprises selectively removing portions of said device structure layer and of said first addressable layer.

41. The method in accordance with claim 40, further comprises selectively etching portions of said device structure layer and of said first addressable layer forming a plurality of logic cells, wherein each nano-rectifying element is substantially facially coextensive, coincident, and coplanar with one of a plurality of first addressable lines and one of said plurality of said nano-storage structures.

42. The method in accordance with claim 28, wherein forming a plurality of self-aligned nano-storage structures further comprises selectively removing portions of said electrically conductive layer, said device structure layer, and said storage media layer.

43. The method in accordance with claim 42, further comprises selectively removing portions of said electrically conductive layer, said device structure layer, and said storage media layer forming a plurality of logic cells, wherein each nano-rectifying element is substantially facially coextensive, coincident, and coplanar with one of a plurality of first addressable lines and one of said plurality of said nano-storage structures.

44. The method in accordance with claim 28, further comprising:

creating a planarizing dielectric layer disposed over said device structure layer, wherein the top surface of said device structure layer forms essentially a plane; and

planarizing said planarizing dielectric layer to substantially said plane of said device structure layer.

45. The method in accordance with claim 28, further comprising: planarizing a dielectric layer disposed over said device structure layer to substantially the same thickness as said plurality of nano-rectifying elements.

46. The method in accordance with claim 28, wherein nano-imprinting said first nano-imprinting layer further comprises removing a recessed portion of said nano-imprinting layer.

47. The method in accordance with claim 28, wherein nano-imprinting said first nano-imprinting layer further comprises creating an etch mask over portions of said nano-imprinting layer and over portions of said device structure layer.

48. The method in accordance with claim 47, further comprising removing said etch mask.

49. The method in accordance with claim 28, wherein forming a plurality of self-aligned nano-rectifying elements further comprises etching said device structure layer.

50. The method in accordance claim 28, further comprising:

creating a storage media layer electrically coupled to said device structure layer; and

creating an electrically conductive layer electrically coupled to said storage media layer.

51. The method in accordance claim 50, wherein creating said storage media layer further comprises creating a storage media layer including a filament forming material.

52. The method in accordance claim 51, wherein said filament forming material is selected from the group consisting of As_2Se_3:Ag, Cu_2S, InSe, and mixtures thereof.

53. The method in accordance claim 50, wherein creating said storage media layer further comprises creating a storage media layer including a organic or polymer material.

54. The method in accordance claim 53, wherein said organic layer further comprises a self-assembled monolayer of organic molecules.

55. The method in accordance claim 50, wherein creating said storage media layer further comprises creating a storage media layer including a piezoelectric material.

56. The method in accordance claim 50, wherein creating said storage media layer further comprises creating a storage media layer including a phase change material.

57. The method in accordance claim 50, wherein creating said storage media layer further comprises creating a storage media layer including a ferroelectric material.